# Reliability Evaluation Plan

## *DPAK package in ASE WEIHAI*

| General Information | |
|---|---|
| **Product Lines** | *LM05* |
| **Product Description** | POSITIVE VR 1.5A 5V |
| **P/N** | *L78M05* |
| **Product Group** | AMG |
| **Product division** | General Purpose Analog & RF POWER MANAGEMENT |
| **Package** | *DPAK* |
| **Silicon Process technology** | *HBIP40V* |

| General Information | |
|---|---|
| **Product Description** | L317 |
| **P/N** | *LM317D2T* |
| **Product Group** | AMG |
| **Product division** | General Purpose Analog & RF POWER MANAGEMENT |
| **Package** | *DPAK* |
| **Silicon Process technology** | *BIP (>6um)* |

| General Information | |
|---|---|
| **Product Description** | KS33 |
| **P/N** | *LD1117* |
| **Product Group** | AMG |
| **Product division** | General Purpose Analog & RF POWER MANAGEMENT |
| **Package** | *DPAK* |
| **Silicon Process technology** | *BIP (>6um)* |

| Locations | |
|---|---|
| **Wafer fab** | *Singapore 6* |
| **Assembly plant** | *ASE WEIHAI* |
| **Reliability Lab** | *Catania Reliability LAB* |

| Version | Date | Pages | Created by | Approved by | Comment |
|---|---|---|---|---|---|
| 1.1 | February-2018 | 5 | Giuseppe Giacopello | Giovanni Presti | First issue |

## DOCUMENT INFORMATION

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods. This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

# TABLE OF CONTENTS

**1 APPLICABLE AND REFERENCE DOCUMENTS ........ 3**
**2 RELIABILITY EVALUATION OVERVIEW ........ 3**
2.1 OBJECTIVES ........ 3
2.2 COSTRUCTION NOTE ........ 3
**3 TEST PLAN ........ 4**
**4 TESTS DESCRIPTION ........ 5**

# 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|---|---|
| **JESD47** | Stress-Test-Driven Qualification of Integrated Circuits |

# 2 RELIABILITY EVALUATION OVERVIEW

## 2.1 Objectives

To qualify the DPAK with cu wires in ASE Weihai.

TV1: KS33 - Maximum Die size
TV2: LM17 - Ag strip on upper side of pad for bonding on frame
TV3: LM05 - Minimum Die size

Three cumulative different qualification Lots are requested
.

## 2.2 Costruction note

| | *KS33* | *LM17* | *LM05* |
|---|---|---|---|
| **Wafer/Die fab. Information** | | | |
| Wafer fab manufacturing location | AMK 6 | AMK 6 | AMK 6 |
| Technology | BIP (>6um) | BIP (>6um) | HBIP40 |
| Die finishing back side | Cr/Ni/Au | Cr/Ni/Au | Cr/Ni/Ag |
| Die size | 1990x1860 | 1990x1810 | 1280x1500 |
| Bond pad metallization layers | AlSi 3µm | AlSi 3µm | AlSiCu |
| Passivation type | SiN | SiN | P-VAPOX/NITRIDE |
| **Assembly information** | | | |
| Assembly site | ASE Weihai | ASE Weihai | ASE Weihai |
| Package description | DPAK | | |
| Mold Compound | Epoxy | | |
| Die attach | Soft solder | | |
| Bond Wire | Copper 1.5 mils | Copper 1.5 mils | Copper 1.5 mils |

# 3 TEST PLAN

| Test | PC | Std ref. | Conditions | | Step | Lot 1 | Lot 2 | Lot 3 | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | LD1117 | LM317 | L78M05 | |
| **Die Oriented Tests** | | | | | | | | | |
| HTOL | N | JESD22 A-108 | Tj = 125° C, BIAS | | 168 H | | 77 | 77 | |
| | | | | | 500 H | | 77 | 77 | |
| | | | | | 1000 H | | 77 | 77 | |
| HTSL | N | JESD22 A-103 | Ta = 150°C | | 168 H | 25 | 25 | 25 | |
| | | | | | 500 H | 25 | 25 | 25 | |
| | | | | | 1000 H | 25 | 25 | 25 | |
| HTSL | N | JESD22 A-103 | Ta = 175°C | | 168 H | 25 | 25 | 25 | Eng |
| | | | | | 500 H | 25 | 25 | 25 | |
| | | | | | 1000 H | 25 | 25 | 25 | |
| **Package Oriented Tests** | | | | | | | | | |
| PC | | JESD22 A-113 | Drying 24 H @ 125°C<br>Store 168 H @ Ta=85°C Rh=85%<br>Oven Reflow @ Tpeak=260°C<br>3 times | | | Final | Final | Final | |
| AC | Y | JESD22 A-102 | Pa=2Atm / Ta=121°C | | 96 h | 25 | 25 | 25 | |
| | | | | | 168 h | 25 | 25 | 25 | Eng |
| TC | Y | JESD22 A-104 | Ta = -65°C to 150°C | | 100cy | 25 | 25 | 25 | (1) |
| | | | | | 200cy | 25 | 25 | 25 | |
| | | | | | 500 cy | 25 | 25 | 25 | |
| THB | Y | JESD22 A-101 | Ta = 85° C, RH = 85%, BIAS | | 168 H | 25 | 25 | 25 | |
| | | | | | 500 H | 25 | 25 | 25 | |
| | | | | | 1000 H | 25 | 25 | 25 | |
| **Other tests** | | | | | | | | | |
| ESD | | JESD22-C101 | CDM | | | Yes | Yes | Yes | |
| CA | | | Construction Analysis | | | Yes | Yes | | |

(1) DPA after 500cy

# 4 TESTS DESCRIPTION

| Test name | Description | Purpose |
|---|---|---|
| **Die Oriented** | | |
| **HTOL**<br>High Temperature Operating Life | The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition. | To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults. |
| **HTSL**<br>High Temperature Storage Life | The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature. | To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding. |
| **Package Oriented** | | |
| **PC**<br>Preconditioning | The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption. | As stand-alone test: to investigate the moisture sensitivity level.<br>As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.<br>The typical failure modes are "pop corn" effect and delamination. |
| **AC**<br>Auto Clave (Pressure Pot) | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature. | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. |
| **TC**<br>Temperature Cycling | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation. |
| **THB**<br>Temperature Humidity Bias | The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity. | To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence. |
| **Other** | | |
| **ESD**<br>Electro Static Discharge | The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models.<br>**CDM**: Charged Device Model | To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge. |
| **CA**<br>Construction Analysis | Construction Analysis | To verify the physical product conformity |